

# How FPGAs Enable Automotive Systems

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## **Overview**

Automotive electronic designs are experiencing a major paradigm shift with shorter design cycles and increasing digital electronic content. Over the next five years, the electronic systems in the automotive space are projected to grow at 7% CAGR, but the pace of PLD (Programmable Logic Device) adoption is projected to grow at a much faster rate of 45% CAGR.

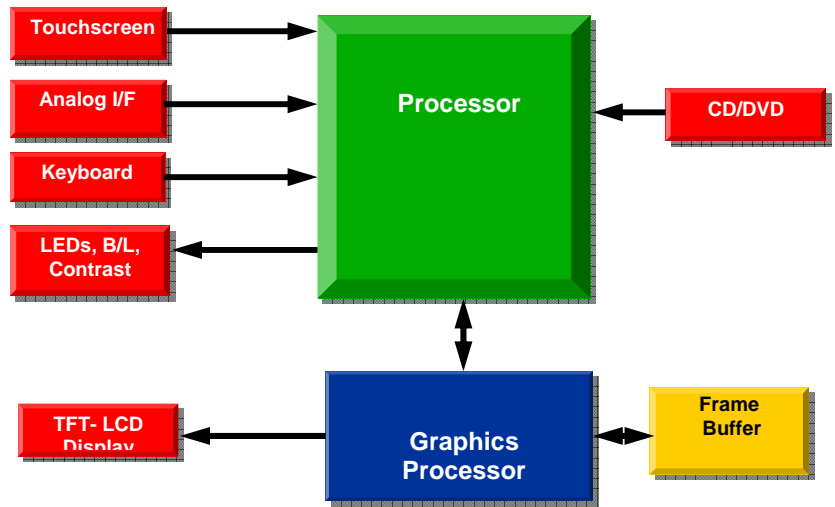
There are several factors driving the adoption of PLDs in the automotive space. First is the evolution of automotive designs toward the “platform” concept, whereby car model differentiation is provided with one basic design. The convergence of audio, video and data in the automotive space is further fueling the platform concept. Second is the fast innovation cycle. Today, a typical automotive design takes approximately 24-36 months, which is much faster than the 60-month life cycle form of five years ago. This short design cycle puts tremendous pressure on system suppliers to quickly prototype and demo their designs to OEMs. Third, increasing digital content in the form of navigation systems, rear seat entertainment systems and driver assistance applications is making its way into the mainstream market. Fourth, ASIC and ASSP suppliers fear product obsolescence, so they are looking to PLDs to provide design flexibility. All of these factors require automotive designers to create a design solution that not only offers superior flexibility, but also meets performance

requirements within their cost targets. Field programmable gate arrays (FPGAs), with their low-cost structure and abundant device resources, provide designers such a solution. This paper will detail the benefits of using FPGAs to implement a high-volume, low-cost solution for the automotive market within multimedia graphics display applications of navigation and rear seat entertainment (RSE) systems.

## **Graphics – Navigation Systems**

Navigation within production systems is one of the key areas in which PLDs have been successfully designed and are now shipping. The system architecture block diagram (Fig. 1) shown is typical of a navigation system, be it a simple turn-by-turn or 2D system. The architecture consists of a host CPU, which is generally a SH4, Power PC, or TI OMAP processor, with a graphics processor. Talking to these processors are various peripherals such as keyboards and TFT displays.

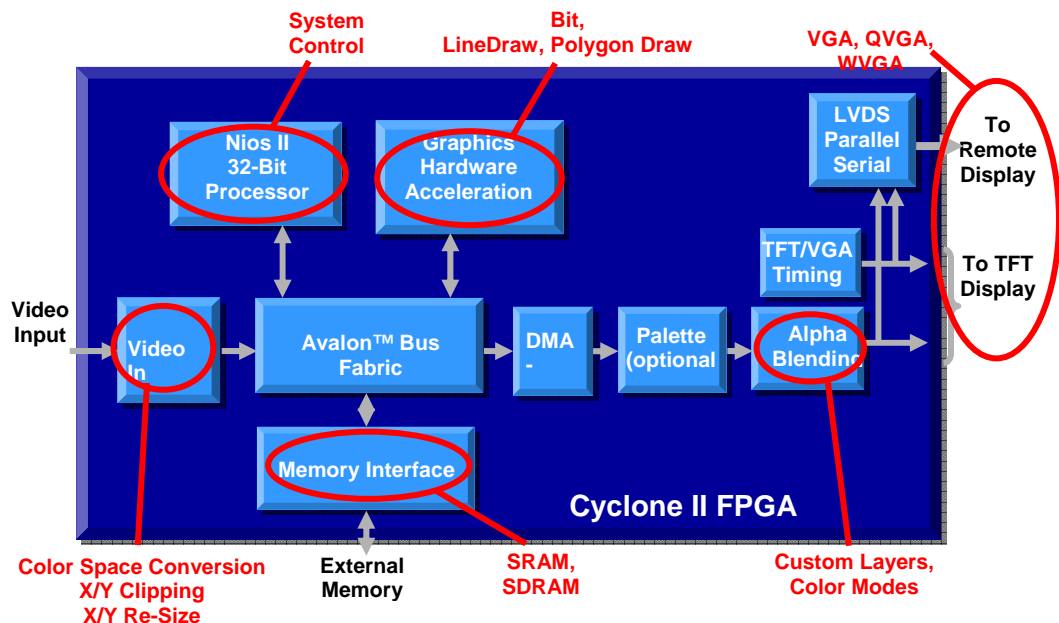
Graphics processing requires the computation of numerous algorithms such as scaling, filtering and alpha blending. FPGAs are better suited than DSPs or ASSPs (application specific standard products) to perform these computationally intensive algorithms because they can handle multiple instructions in a single clock cycle.



**Figure 1: Typical Navigation System**

Figure 2 shows a low-cost graphics implementation in an Altera Cyclone II FPGA. The video-in could be BT.656 input (YUV 4:2:2), with color space converter (CSC) to output RGB. The memory interface to the Avalon bus fabric allows high graphic computations to be accommodated. Memory type that can be supported includes SRAM, SDRAM and DDR-SDRAM. Nios II is Altera's 32-bit embedded processor, which is primarily

used for graphics processing (line draw, frame creation) and to provide other control functions. Graphics hardware acceleration could include functions such as BitBlt (copy object into frame buffer, 2D-DMA transfer, possibly with blending). Alpha blending can have multiple channels. Cyclone II is capable of supporting LVDS graphics output for remote display applications.



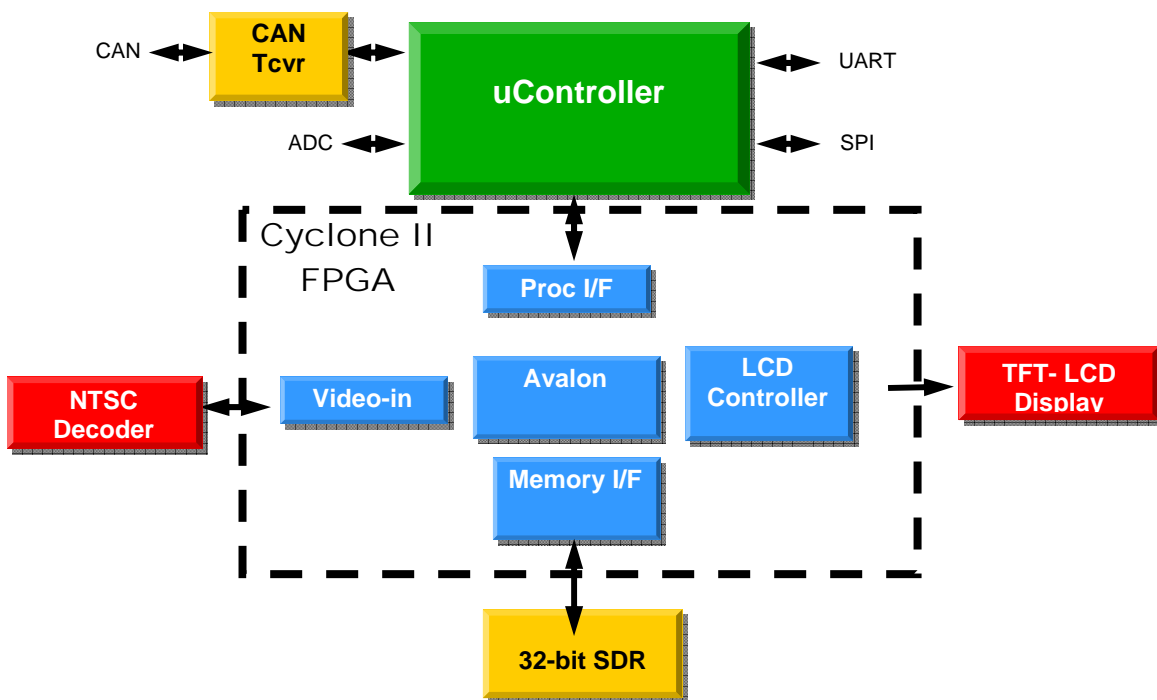
**Figure 2: Low Cost Graphics Implementation Using Cyclone II FPGA (EP2C5)**

## Graphics – Rear Seat Entertainment

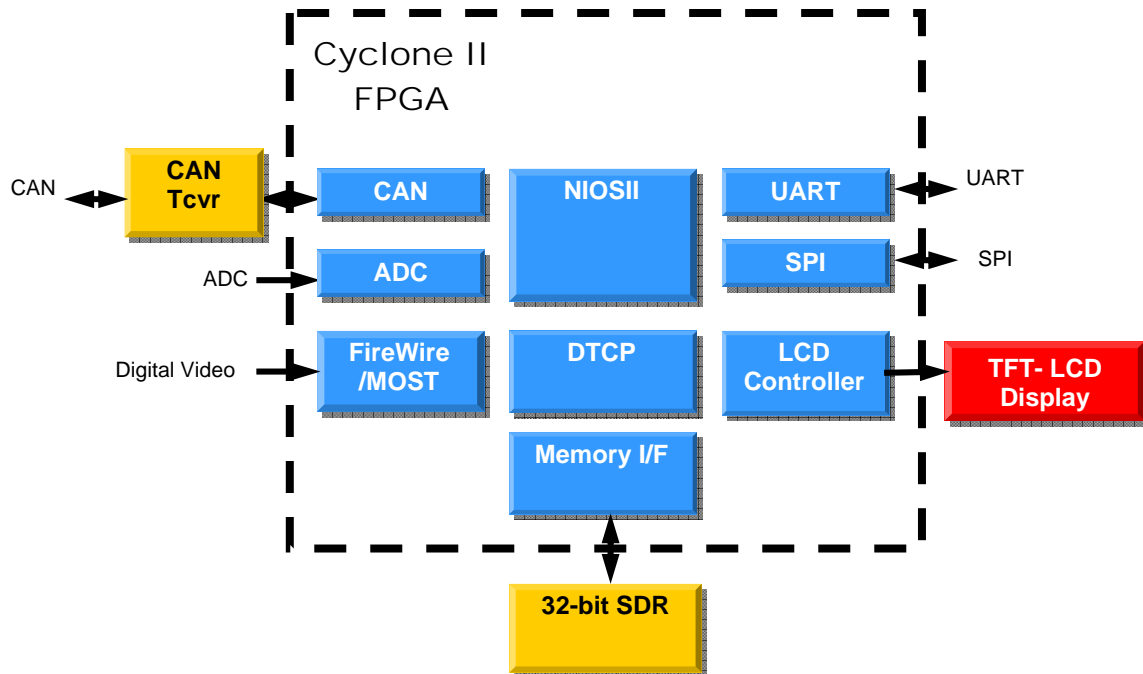
Rear Seat Entertainment (RSE) is one of the emerging areas where PLDs have been widely adopted. Like navigation systems, RSE systems involve a significant amount of graphics processing, especially as it relates to video quality. Figure 3 shows a typical current RSE system. The key components are the microcontroller (uC), FPGA, memory, other ASSPs and peripherals. The uC is typically 16-bit or 32-bit. The ASSPs usually include functionalities such as decoding and Controller Area Network (CAN) transceivers.

Next generation RSE systems look quite different from the current ones. Designers are being forced to lower their BOM cost and look for ways to make the system more flexible,

whereby they can target high-range, mid-range and low-range platforms. One way to achieve this is by integrating some of the ASSP functionalities onto the existing FPGA. As shown in figure 4, the uC functionality has been absorbed by the FPGA, in this case provided by Altera's 32-bit Nios II RISC processor. The CAN interface can easily be supported within the FPGA, consuming less than 10% of the Cyclone II EP2C8 device. Besides the CAN interface, the FPGA can also support the Media Oriented System Transport (MOST) Media LB Interface. MOST is the next generation optical-based interface that is widely being adopted for next generation infotainment and communication systems. For areas where MOST does not make sense, Firewire offers a viable option.



**Figure 3: Current Rear Seat Entertainment (RSE) Implementation (EP2C5)**



**Figure 4: Next Generation Rear Seat Entertainment (RSE) Implementation (EP2C8)**

In addition to absorbing ASSP functionalities, the FPGA has an ample amount of room to do video processing. With an on-chip MOST or Firewire interface, the FPGA can easily support digital video mode, giving system suppliers added feature differentiation from the competition. This system integration not only lowers the overall system cost, but also provides system suppliers more flexibility to add additional functionalities.

**Automotive Graphics Reference Design**

The Automotive Graphics System reference design demonstrates the use of Altera Cyclone™ FPGAs in a graphics system, which can be used for either a navigation or RSE type of application. This reference design shows the power and flexibility available in FPGAs for targeting low-cost applications.

The main reference design features are:

- Video input hardware module
  - Clipping

- Color space conversion
- Horizontal and vertical scaling
- TFT display controller
  - 5-layer display
  - Picture in picture
- Graphics library running on Nios® II processor
- Runs on Nios II Cyclone development board
  - Lancelot VGA video controller required
- SDRAM program store and frame buffer

This reference design is available at no cost and can be downloaded from Altera’s web site.

**Conclusion**

The automotive industry is beginning to take a hard look at how FPGAs can contribute to the success of both system suppliers and automakers (OEMs). Several years ago the use of FPGAs was unheard of in the automotive space. However, with lowering cost structure and increasing system

performance, FPGAs are now making their way into the mainstream automotive market. With the increasing usage of electronics in the automotive industry, the use of FPGAs is going to increase. Unlike ASSP solutions, FPGAs provide flexibility that is an ever increasing requirement in the automotive industry. PLDs, which have already found a home in the infotainment and communications markets, now are making

their way into the emerging driver assistance automotive segment, which consists of some of the fastest growing applications such as lane departure warning, night vision and tire pressure monitoring. With a low silicon cost structure, abundance of IP cores, reference designs and long product shelf life, PLDs will be a force to be reckoned with in the growing automotive electronics market.



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