

This document addresses known errata and documentation changes for DSP Builder version 6.0 SP1. Errata are functional defects or errors which may cause DSP Builder to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.

DSP Builder v6.0 SP1 Issues

There are no new issues in DSP Builder, version 6.0 (SP1). However, the MATLAB Fixed Point License Error and Wrong Library Directory in Verilog Testbench TCL Scripts issues have been fixed.

DSP Builder v6.0 Issues

Table 1 shows the issues that affect DSP Builder, version 6.0.

<i>Table 1. DSP Builder v6.0 Issues</i>	
Issue	Page
Tcl Scripts Generated for VIP MegaCore Functions	1
MATLAB Fixed-Point License Unnecessarily Checked Out	2
Wrong Library Directory in Verilog Testbench Tcl Scripts	3
Multiclock Designs May Not Simulate Correctly in ModelSim	3
Signed Fractional HIL Simulation is Incorrect	4
Unique Entity Names Option Cannot be Unset	4
VHDL for Black Box Not in Generated Scripts	5
Previous DSP Builder Path Not Removed	5



For the most up-to-date errata for this release, refer to the errata page on the Altera website:

www.altera.com/literature/es/es_dsp_builder_60.pdf

Altera has identified the following issues in DSP Builder version 6.0.

Tcl Scripts Generated for VIP MegaCore Functions

The IP Toolbench generated Tcl files for Video and Image Processing Suite MegaCore functions do not include all the generated VHDL.

Affected Configurations

Configurations that use Video and Image Processing Suite MegaCore functions.

Design Impact

DSP Builder cannot locate the VHDL files generated by IP Toolbench and compilation using the Quartus II software in the SignalCompiler flow fails.

Workaround

Edit the `<variation_name>_add.tcl` script that can be found in the `DSPBuilder_<design_name>` directory and add a line that sources the `vip_setup.tcl` script in this directory. For example, if the design name is `viptest` and is located at `D:/mydesign`, add the line:

```
source "D:/mydesign/DSPBuilder_viptest/vip_setup.tcl"
```

Solution Status

This issue will be fixed in a future release of the Video and Image Processing Suite.

MATLAB Fixed-Point License Unnecessarily Checked Out

Changes have been made which would require a fixed point license and DSP Builder unnecessarily attempts to check out this license by default.

Affected Configurations

Configurations that do not have access to a fixed-point MATLAB license.

Design Impact

Errors are reported if you do not have a MATLAB fixed-point license and initialization commands cannot be evaluated.

Workaround

Contact Altera customer support for a patch build which resolves this issue.

Solution Status

This issue will be fixed in DSP Builder 6.0 SP1.

Wrong Library Directory in Verilog Testbench Tcl Scripts

The library directory for `convert_hex2ver.dll` is incorrect in the testbench Tcl scripts for version 6.0.

Affected Configurations

All configurations are affected.

Design Impact

The wrong library directory is referenced in the Tcl scripts.

Workaround

Edit the `tb_vo_<design_name>.tcl` file and change the location where simulation is loaded from `$megadir` to `$libdir`, as shown by the following example:

```
# load simulation
vsim -pli "$megadir/convert_hex2ver.dll" -t $TimeResolution work.tb_singen

# load simulation
vsim -pli "$libdir/convert_hex2ver.dll" -t $TimeResolution work.tb_singen
```

Solution Status

This issue will be fixed in a future release of DSP Builder.

Multiclock Designs May Not Simulate Correctly in ModelSim

Some multiclock designs may not simulate correctly in ModelSim.

Affected Configurations

All configurations are affected.

Design Impact

When a design involves a clock rate change from low to high, the `.salt` file could be in the lower rate clock domain. If the outputs to be monitored are in the high clock rate domain, the `.salt` file will be misinterpreted in the testbench causing simulation in ModelSim to be incorrect.

Workaround

None.

Solution Status

This issue will be fixed in a future release of DSP Builder.

Signed Fractional HIL Simulation is Incorrect

HIL signed fractional simulation does not match the non-HIL simulation

Affected Configurations

All configurations are affected.

Design Impact

HIL simulation matches the non HIL simulation in a signed integer design but does not match in a signed fractional version of the design.

Workaround

The HIL (and HDL Import) blocks require integer inputs and outputs. Insert Binary Point Casting blocks at the inputs and outputs to convert between signed fractional and integer.

Solution Status

This issue will be fixed in a future release of DSP Builder.

Unique Entity Names Option Cannot be Unset

The option in SignalCompiler to generate unique hierarchical names cannot easily be unset.

Affected Configurations

All configurations are affected.

Design Impact

When running SignalCompiler, the analyze stage has a check box for **Hierarchical VHDL entity names are unique**. Once turned on, this setting can not be easily turned off, as it makes changes to the model.

Workaround

The unique names option has been disabled in version 5.1. However, it can be enabled by setting the following MATLAB workspace variable:
`dspbuilder_enable_unique_hierarchy_name = true;`

Solution Status

This issue will be fixed in a future release of DSP Builder.

VHDL for Black Box Not in Generated Scripts

The VHDL source code for black box blocks is not included in the generated scripts.

Affected Configurations

All configurations are affected.

Design Impact

When SignalCompiler generates Tcl scripts for the Quartus® II software and all 3rd party synthesis and simulation tools, the VHDL source code for the top level is included. However, VHDL source code for any black boxes in the design is not included.

Workaround

Manually edit the Tcl scripts to include VHDL source code for all black box sources in the design. If any VHDL source refers to any special libraries, those libraries also need to be included with appropriate compiler directives.

Solution Status

This issue will be fixed in a future release of DSP Builder.

Previous DSP Builder Path Not Removed

If DSP Builder version 5.0 has been previously installed then its path will not be removed from the MATLAB path list when DSP Builder version 5.0 is un-installed.

Affected Configurations

Configurations which have been updated from DSP Builder version 5.0.

Design Impact

Error messages are issued due to library objects existing at more than one location.

Workaround

The DSP Builder path for version 5.0 was written to a **startup.m** file in the MATLAB installation (for example: *<MATLAB install directory> \toolbox\local\startup.m*). You should manually comment out (using the % character) or remove the DSP Builder path specified in this file. For example:

```
%path(path, 'C:\altera\DSPBuilder\AltLib');
```

Solution Status

This issue will be fixed in a future release of DSP Builder.

Contact Information

For more information, contact Altera's mySupport website at www.altera.com/mysupport and click **Create New Service Request**. Choose the **Product Related Request** form.

Revision History

Table 2 shows the revision history for the *DSP Builder 6.0 SP1 Errata Sheet*.

Version	Date	Errata Summary
1.4	June 2006	Updated for software version 6.0 SP1.
1.3	June 2006	Added errata for “ Tcl Scripts Generated for VIP MegaCore Functions ”.
1.2	May 2006	Added errata for “ MATLAB Fixed-Point License Unnecessarily Checked Out ”.
1.1	May 2006	Added errata for “ Wrong Library Directory in Verilog Testbench Tcl Scripts ”.
1.0	April 2006	New document for DSP Builder 6.0.



101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
www.altera.com
Applications Hotline:
(800) 800-EPLD
Literature Services:
literature@altera.com

Copyright © 2006 Altera Corporation. All rights reserved. Altera, The Programmable Solutions Company, the stylized Altera logo, specific device designations, and all other words and logos that are identified as trademarks and/or service marks are, unless noted otherwise, the trademarks and service marks of Altera Corporation in the U.S. and other countries. All other product or service names are the property of their respective holders. Altera products are protected under numerous U.S. and foreign patents and pending applications, maskwork rights, and copyrights. Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera Corporation. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.

